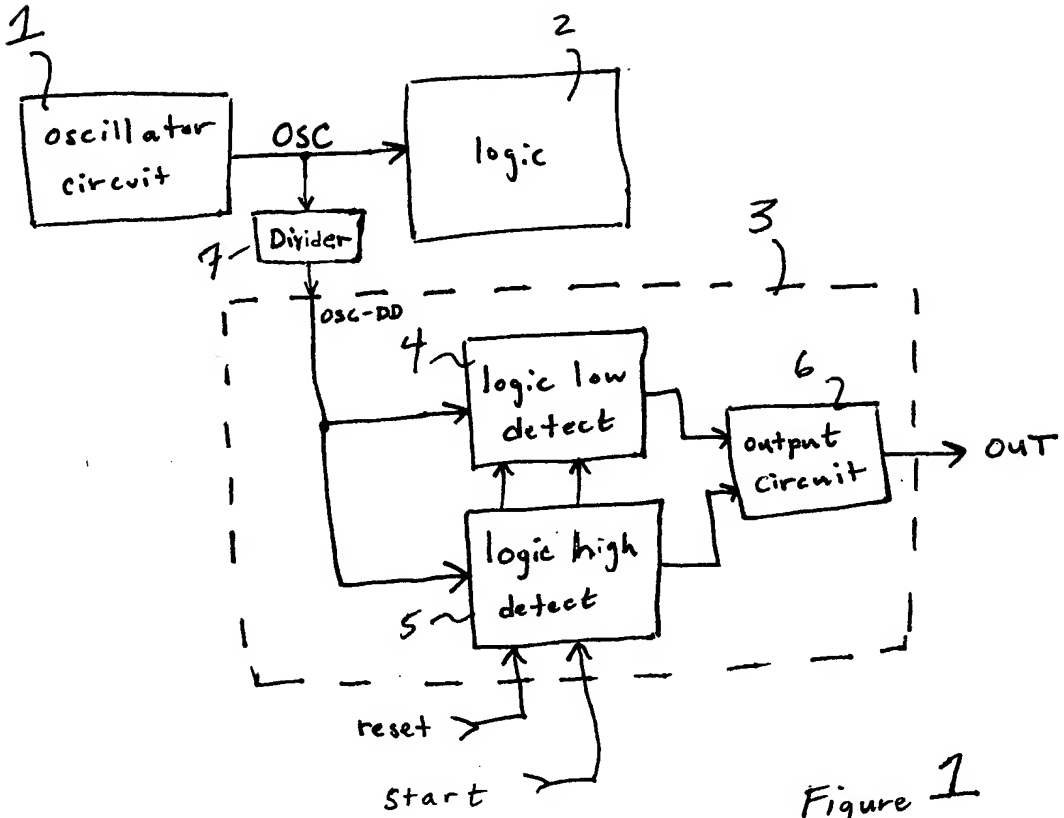
1
oscillator circuit
OSC
2
logic
Divider
7
3
OSC-DD
4
logic low detect
6
output circuit
OUT
logic high detect
5
reset
Start

Figure 1

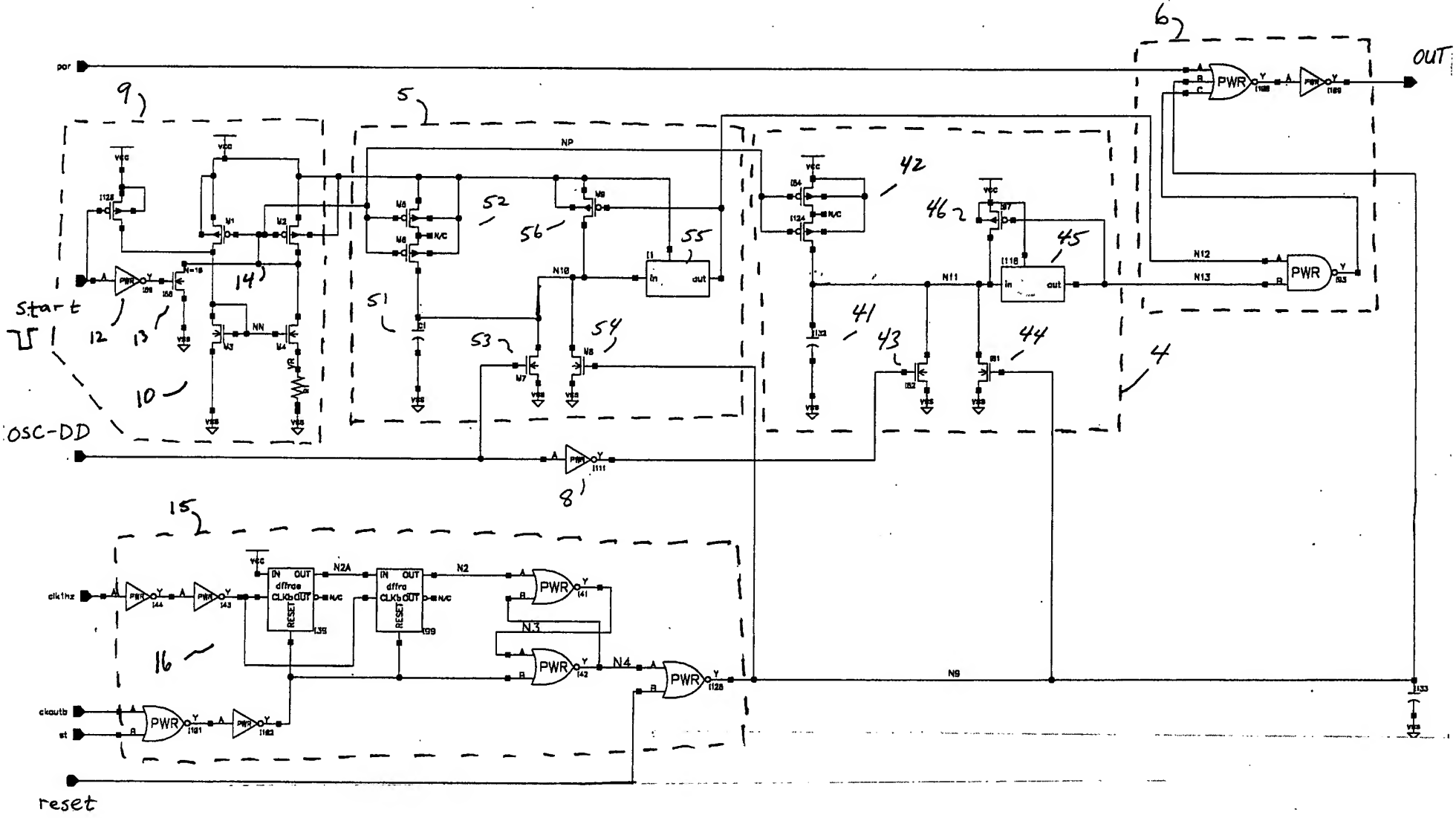
3
6
OUT
por
9
5
NP
42
52
56
55
46
45
N12
N13
N18
N11
start
12
13
14
51
41
53
54
43
44
4
10
OSC-DD
8
15
clk1hz
N2A
N2
N3
N4
16
N9
ckoutb
st
reset

Figure 2

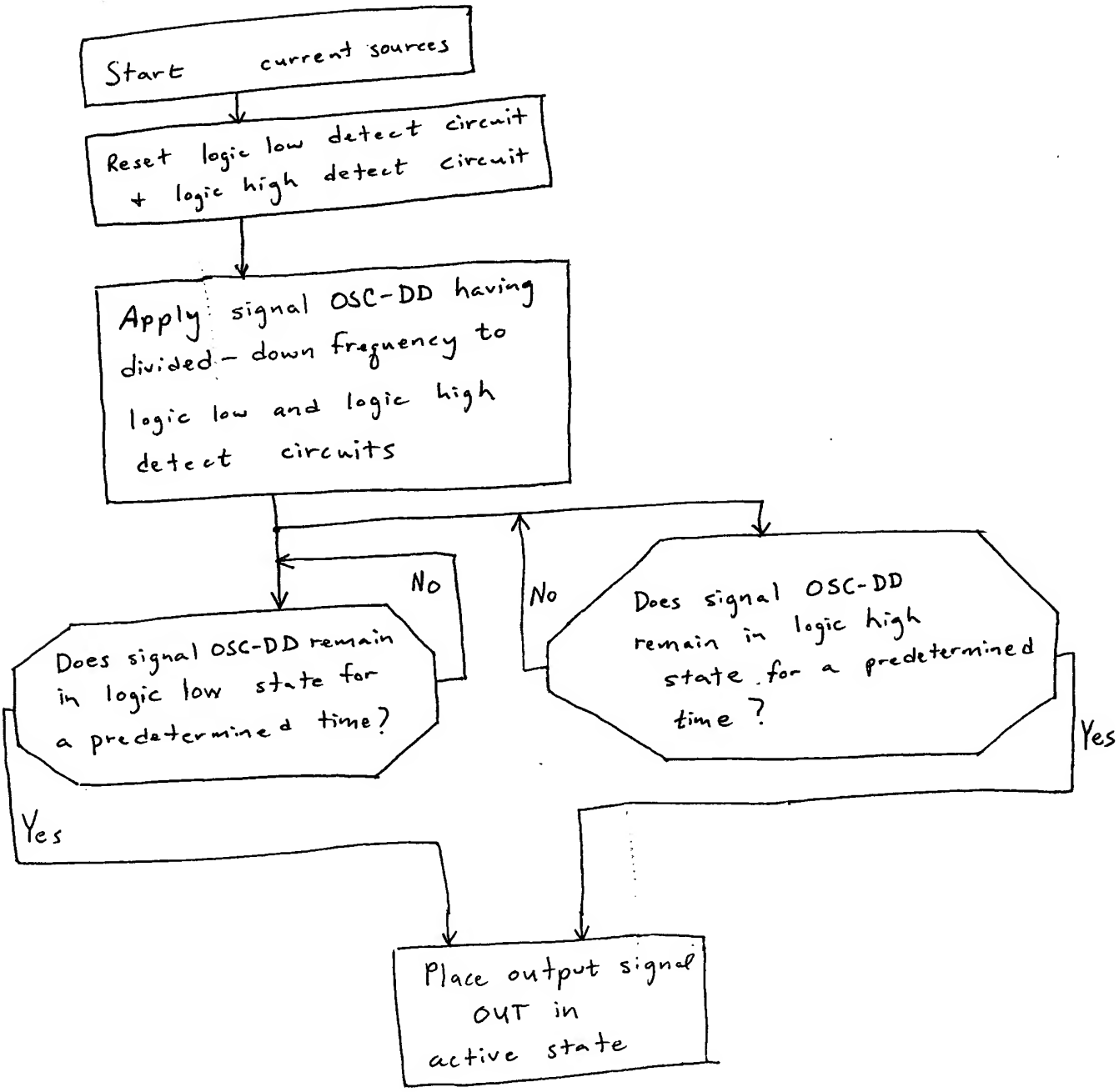
Start current sources
Reset logic low detect circuit + logic high detect circuit
Apply signal OSC-DD having divided-down frequency to logic low and logic high detect circuits
Does signal OSC-DD remain in logic low state for a predetermined time?
No
Yes
Does signal OSC-DD remain in logic high state for a predetermined time?
No
Yes
Place output signal OUT in active state

Figure 3